ABSTRACT OF THE DISCLOSURE.

A vertical nano-transistor having a source region, a drain region, a gate region and a semiconductor channel region between the source region and the drain region, the gate region being constituted by a metal film into which the transistor is embedded in such a manner that the gate region and the semiconductor channel region form a coaxial structure, the source region, the semiconductor channel region and the drain region being disposed vertically, and the gate region being electrically insulated from the source region, the drain region and the semiconductor channel region. The invention also relates to a method of producing the inventive transistor and a memory assembly.